ABSTRACT OF THE DISCLOSURE

A system and method for producing a fused instruction is described. In one embodiment, a first instruction and a second instruction that are both simple instructions (e.g., perform only one operation) and are dependent are fused together to create the fused instruction. The fused instruction has an opcode that represents the operation performed by the first instruction and the operation performed by the second instruction. The fused instruction has three source operands and one destination operand. Two of the three source operands are the two source operands of the first instruction, and the third source operand is the source operand of the second instruction that is not the destination operand of the first instruction. The destination operand of the fused instruction is the destination operand of the second instruction. An execution unit that can execute a fused instruction in one clock cycle is also disclosed. In one embodiment, the execution unit has two arithmetic logic units ("ALUs"), each of the ALUs performs one of the two operations of the fused instruction. The result of the first ALU is input into the second ALU to produce the desired result.